DRONACHARYA COLLEGE OF ENGINEERING

KHENTAWAS, FARRUKHNAGAR, GURGAON, HR

Department: EEE

Academic Session: 2020-2021(MAY- AUG, 2021)

Lecture Plan with Asssignment questions

Subject with code: Electromagnetic Field(PCC-EE-216-G)

Name of Faculty with designation : Dr. Ekta Thakur, Assistant Professor

S.No.	Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Write Lecture Wise Questions
1	May	1	IV EEE	I	Introduction of MOS Transistor,MOS Transistor, CMOS logic, .	Q1) Question related to mos Q2) Question related to CMOS
2	May	2	IV EEE	I	Layout Design Rules, Gate Layouts,	Q1) Question related to NOR,OR Truth tables Q2) Question related to design
3	May	3	IV EEE	I	Stick Diagrams, Long-Channel I-V characteristics,	Q1) Question related toIV Charateristics Q2) Question related to diagram
4	June	4	IV EEE	I	C-V characteristics, Non ideal I-V Effects,	Q1) Question related to I-V Effect Q2) Question related toC-V characteristic
5	June	5	IV EEE	I	Elmore Delay	Q1) Question related to delay Q2) Question related to delay
6	June	6	IV EEE	I	Linear Delay Model	Q1) Question related to linear Q2) Question related to delay
7	June	7	IV EEE	I	Logical effort	Q1) Question related logical effort Q2) Question related to array
8	June	8	IV EEE	I	Parasitic Delay	Q1) Complexity analysis of parastic delay Q2) Complexity analysis of delay
9	June	9	IV EEE	I	Delay in Logic Gate,Scaling.	Q1) Complexity analysis of scaling Q2) Complexity analysis ofgates
10	June	10	IV EEE	II	Combinational Circuit Design,Circuit Families:	Q1) Complexity analysis of various circuits Q2) Applications of design
11	June	11	IV EEE	II	Static CMOS,	Q1) Complexity analysis of cmos Q2) Applications of Static

12	June	12	IV EEE	I	Ratioed Circuits	Q1) Complexity analysis of cmos Q2) Applications of Static
13	July	13	IV EEE	I	Cascode Voltage Switch Logic	Q1) Numerical Q2) Numerical
14	July	14	IV EEE	I	Dynamic Circuits, Pass Transistor Logic	Q1) Numerical Q2) Numerical
15	July	15	IV EEE	II	Transmission Gates	Q1) Complexity analysis of gate Q2) Complexity analysis ofgates
16	July	16	IV EEE	II	Domino, Dual Rail Domino	Q1) Numerical Q2) Numerical
17	July	17	IV EEE	II	CPL, DCVSPG,DPL, Circuit Pitfalls	Q1) Numerical Q2) Numerical
18	July	18	IV EEE	II	Power: Dynamic Power, Static Power	Q1) Numerical Q2) Numerical
19	July	19	IV EEE	II	Low Power Architecture	Q1) Numerical based on deletion operation Q2) Comparison of various operations using linked list and array
20	July	20	IV EEE	II	Interconnect: Interconnect Modelling and Impact	Q1) Question related architecture Q2) Question related to power
21	July	21	IV EEE	III	equential Circuit Design Static latches and Registers Dynamic latche	Q1) Question related seqentail circuits Q2) Question related to latches
22	July	22	IV EEE	III	Registers, Pulse Registers	Q1) Numerical Q2) Numerical
23	August	23	IV EEE	III	Pipelining,	Q1) Numerical Q2) Numerical
24	August	24	IV EEE	III	Schmitt Trigger,Monostable Sequential Circuits,	Q1) Numerical Q2) Numerical
25	August	25	IV EEE	III	Astable Sequential Circuits	Q1) Question related astable Q2) Question related to circuits
26	August	26	IV EEE	III	Timing Issues: Timing Classification of Digital System,	Q1) Numerical Q2) Numerical
27	August	27	IV EEE	III	Modeling of Coupled Electromechanical Systems:	Q1) Numerical Q2) Numerical
28	August	28	IV EEE	IV	Implementation of of simple microcomputer system	Q1) Numerical Q2) Numerical
29	August	29	IV EEE	IV	Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs	Q1) Question related multipliers Q2) Question related to shifters

30	August	30	IV EEE	IV	Case Study: Design as a tradeoff,Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry	Q1) Complexity analysis of tradeoff,architectures